IMAGE-PROCESSING DEVICE, IMAGE-PROCESSING METHOD AND SOLID-STATE IMAGE PICKUP DEVICE

Related Applications

[0001] The entire disclosure of Japanese Patent Application No. 2003-013603 filed January 22, 2003 is hereby incorporated by reference in its entirety.

Background of the Invention

[0002] Technical Field of the Invention

[0003] The present invention relates to an image-processing device, an image-processing method and a solid-state image pickup device. In particular, the invention relates to an image-processing device that picks an image up with a solid-state image-pickup element, an image-processing method and a solid-state image pickup device thereof.

[0004] Description of the Related Art

[0005] A semiconductor image sensor is used for various kinds of image input devices. Recently, of such semiconductor image sensors, a MOS solid-state image-sensing device with a threshold voltage modulation system attracts attention since it provides high image quality attained by a CCD (charged coupled device) with low power consumption by a CMOS and restrains deterioration of an image quality and realizes high density and low cost.

[0006] Technology of a MOS solid-state image-sensing device with a threshold voltage modulation system is disclosed in the Japanese Patent Publication Laid-Open No. 11-195778 for example. In a MOS solid-state image-sensing device with a threshold voltage modulation system, three states such as initialization, accumulation and reading out are repeated such that an image signal based on charges for emitting light that are accumulated in a carrier pocket of each pixel can be pulled out. An initialization period is a period of discharging residual charges from a carrier pocket. An accumulation period is a period of accumulating charges in a sensor cell. A reading out period is a period of reading a volume of charge out with voltage modulation.

[0007] However, for example, if the gate voltage is boosted in order to increase a ratio of selected lines while in the state of an accumulation period for

accumulating photo generated charges in a carrier pocket to non selected lines while in the sate of a reading out period for reading an image signal based on accumulated photo generated charges, holes are not selected sufficiently so as not to obtain good image quality.

[0008] However, the Japanese Patent Publication Laid-Open No. 11-195778 does not disclose a method of applying a gate voltage in order to obtain a good image quality in such case.

[0009] Therefore, the present invention is intended to provide an image-processing device that applies a gate voltage in order to obtain a good image quality, an image-processing method and a solid-state image pickup device thereof .

Summary

[0010] An image-processing device of the present invention comprises: a solid-state image pickup element provided with a plurality of unit pixels each including a photo diode and a plurality of transistors for detecting an optical signal. Further, the device comprises a circuit for changing a gate-applied voltage that changes a voltage applied to each gate of a plurality of the transistors; a first voltage source coupled to the circuit for changing gate-applied voltage; and a second voltage source coupled to the circuit for changing gate-applied voltage. In this device, the circuit for changing a gate-applied voltage applies a predetermined voltage to each gate of a plurality of the transistors from the first voltage source while in the accumulation state when carriers are generated from the photo diode in response to received light, and/or applies another predetermined voltage from the second voltage source while in the reading out state when a signal in response to carriers accumulated in the accumulation state is read out.

[0011] A method of image processing of the present invention that picks an image up with a solid-state image pickup device provided with a plurality of unit pixels each including a photo diode and a plurality of transistors for detecting an optical signal, comprises: applying a predetermined voltage to each gate of a plurality of the transistors from a first voltage source while in the accumulation state when carriers are generated from the photo diode in response to received light, and applying a predetermined voltage to each gate of a plurality of the transistors from a second voltage while in the reading out

state when a signal in response to carriers accumulated in the accumulation state is read out.

[0012] A solid-state image pickup device of the present invention comprises: a solid-state image pickup element provided with a plurality of unit pixels each including a photo diode and a plurality of transistors for detecting an optical signal, a circuit for changing gate-applied voltage that changes a voltage applied to each gate of the plurality of transistors and a regulator that produces a first voltage and a second voltage In this device; the circuit for changing a gate-applied voltage applies the first voltage that output from the regulator to each gate of a plurality of the transistors while in the accumulation state when carriers are generated from the photo diode in response to received light, and/or applies the second voltage that output from the regulator to each gate of a plurality of the transistors while in the reading out state when a signal in response to carriers accumulated in the accumulation state is read out.

[0013] According to such structure, an image-processing device supplying a gate voltage can be realized to obtain a good image quality.

[0014] Furthermore, an image-processing device of the present invention comprises a third voltage source coupled to the circuit for changing gate-applied voltage. In the device, the circuit for changing gate-applied voltage applies a predetermined voltage to each gate of a plurality of the transistors from the third voltage source while in the clearing state when the carriers maintaining in the solid-state image pickup device are excluded from the solid-state image pickup device.

[0015] The image-processing device of the present invention may further comprise a plurality of gate voltage supplying circuits wherein the changed applied voltage is applied to a plurality of the gate voltage supplying circuits from the circuit for changing gate-applied voltage.

[0016] The image-processing device of the present invention may further comprise a plurality of gate voltage supplying circuits wherein a plurality of the gate voltage supplying circuits include the circuit for changing a gate-applied voltage.

Brief Description of the Drawings

[0017] FIG. 1 is a block diagram showing a structure of an image-processing device related to the preferred embodiment of the present invention.

[0018] FIG. 2 is a circuit diagram showing a structure of an image sensor LSI related to the preferred embodiment of the present invention.

[0019] FIG. 3 is a circuit diagram showing a structure of a drain gate voltage supply circuit related to the preferred embodiment of the present invention.

[0020] FIGS. 4A and 4B are circuit diagrams showing a structure of a source voltage supply circuit related to the preferred embodiment of the present invention.

[0021] FIG. 5 is a diagram explaining a bias voltage applied to a sensor cell related to the preferred embodiment of the present invention.

[0022] FIG. 6 is a diagram explaining a line for reading out an image signal and a line for clearing an image signal of a sensor of the preferred embodiment of the present invention.

[0023] FIG. 7 is a timing chart showing timing chart of a vertical synchronizing signal and a horizontal synchronizing signal related to the preferred embodiment of the present invention.

[0024] FIG. 8 is a circuit block diagram showing a structure of a timing generator of an image sensor LSI related to the preferred embodiment of the present invention.

[0025] FIG. 9 is a timing chart explaining a state of each signal in each state within a H blanking period related to the preferred embodiment of the present invention.

[0026] FIG. 10 is a diagram showing a modified example of a drain gate voltage applying circuit.

Detailed Description

[0027] The preferred embodiments of the present invention are explained in detail referring to the drawings.

[0028] At first, an overall structure of an image-processing device related to the present embodiments is explained referring to FIG. 1.

[0029] FIG. 1 shows a block diagram of the image-processing device comprising an image sensor LSI (large scale integrated circuit) 1 as a solid-state image pickup device and a signal-processor LSI 2 as a signal-processing device. The image sensor LSI 1 is a two-dimensional solid-state image pickup device that converts an optical image to an electrical signal and applies this pixel signal based on the optical image to the signal-processor LSI 2. The

signal-processor LSI 2 implements a predetermined signal processing to each of received pixel signals and outputs an image signal.

[0030] The image sensor LSI 1 includes a sensor cell array 3, a second shift register 4, a first shift register 5 and a vertical drive circuit 6 and a booster 7, a regulator 8, a line memory 9 for an accumulated signal, a line memory 10 for an offset signal, a horizontal shift register 11, an output amplifier 12 and a timing generator 13. The timing generator 13 includes a register 14 and a three line serial interface 15. The second shift register 4 is connected to a line for clearing an image signal and the first shift register 5 is connected to a line for reading out an image signal.

[0031] For example, the sensor cell array 3 in the image sensor LSI 1 is a solid-state image pickup device with the threshold modulation system disclosed in the Japanese Patent Publication Laid-Open No. 11-195778. Various control signals are applied to various circuits from the timing generator 13. Based on these control signals, the sensor cell array 3 outputs pixel signals according to an amount of light that each cell receives. In addition, for example, the sensor cell array 3 includes cells of 640x480 and a region for optical black (OB or an OB region). When it includes cells and the OB region, the sensor cell array 3 comprises cells of 712x500, for example. Further, the image sensor LSI 1 applies two output signals such as an analog output signal VOUTS, which is a signal component in response to an amount of received light, and an analog output signal VOUTN in response to an offset component, to the signal-processor LSI 2.

[0032] The vertical drive circuit 6 is a circuit for selecting a line for reading out an image signal and a line for clearing an image signal. The first shift register 5 and the second shift register 4 are circuits that designate a line for reading out an image signal and a line for clearing an image signal respectively.

[0033] The regulator 8 is a voltage production circuit for producing various voltages applied to components in the image sensor LSI 1. The booster 7 is a circuit that boosts voltages applied from the regulator 8 in order to apply necessary voltages to the sensor cell array 3 described below. In addition, the image sensor LSI 1 will be explained in detail referring to FIG.2.

[0034] The signal-processor LSI 2 includes a differential amplifier 16, an optical black (abbreviated with OB hereafter) clamping circuit 17 and a programmable gain amplifier (PGA) 18 and an analog to digital conversion

circuit (ADC) 19, an OB control logic circuit 20, a brightness control logic circuit 21, a brightness measurement logic circuit 22, a register 23, an image processor 24, a sequencer 25 and a timing generator 26. The register 23 stores data such as shutter speed data and others.

[0035] Two analog signals such as the voltage output signals VOUTS and VOUTN from the image sensor LSI 1 are input into the differential amplifier 16. The differential amplifier 16 of the signal-processor LSI 2 takes the difference between a voltage value of the signal component and a voltage value of the offset component, amplifies and outputs such difference to the OB clamping circuit 17.

[0036] The OB clamping circuit 17 is a circuit that sets a black level of an input pixel signal to an appropriate black level. A cell including predetermined several numbers of pixels within the sensor cell array 3, namely an OB area, is shielded by a light shield and others. Based on the signal level from the shielded cell, an appropriate black level can be arranged with respect to pixel signals in a valid pixel region.

[0037] The PGA 18 is an amplifier that adjusts a gain by 1db. unit, for example. A signal amplified by the PGA 18 is applied to the ADC 19. The ADC 19 converts the output of the PGA 18 to a digital signal. Data regarding the brightness of pixels located in the OB region is applied to the OB control logic circuit 20 as a digital signal from the ADC 19. The OB control logic circuit 20 receives a signal from the ADC 19 based on a control signal from the timing generator 26 and outputs a control signal to the OB clamping circuit 17 in order to adjust a black level.

[0038] Similarly, the brightness measurement logic circuit 22 measures the brightness based on all data of green (G) pixels within one frame supplied from the ADC 19, for example and applies the brightness data to the brightness control logic circuit 21.

[0039] The brightness control logic circuit 21 applies a gain control signal to the PGA 18 so as to adjust the brightness of an image based on the brightness data applied from the brightness measurement logic circuit 22. Furthermore, the brightness control logic circuit 21 writes data of a shutter speed in the register 23.

[0040] In addition, the register 14 and the register 23 store the same data as each other. Thus, if the content in one of these registers is changed, the content in the other of these registers is also changed via the three line

serial interface 15. Therefore, when the data of a shutter speed is written in the register 23 of the signal-processor LSI 2, such data is further transferred and written in the register 14 of the image sensor LSI1 via the three line serial interface 15. In the image sensor LSI 1, the focal plane shutter is set based on the data of a shutter speed. The function of the focal plane shutter is described below.

[0041] The image sensor LSI 1 controls the width "d1" between a line for reading out an image signal and a line for clearing an image signal of the focal plane based on the data of a shutter speed, for example. When an image is bright and exposure time is shortened, it controls the narrowing of the width "d1", namely decreasing the number of lines between a line for reading out an image signal and a line for clearing an image signal. In addition, when an image is dark and exposure time is lengthened, it controls the broadening of the width "d1", namely increasing the number of lines between a line for reading out an image signal and a line for clearing an image signal. Furthermore, when exposure is not great enough only by controlling a shutter speed, the brightness control logic circuit 21 controls the signal gain so as to adjust appropriate signal amounts.

[0042] A system clock signal CLKIN is applied to the signal-processor LSI 2. The timing generator 26 in it produces various timing signals based on the system clock signal CLKIN. The signal-processor LSI 2 applies various kinds of synchronizing signals among various kinds of timing signals to the image sensor LSI 1. As a synchronizing signal, there are a sensor drive clock signal SCLK, a vertical synchronizing signal VSYNC and a horizontal synchronizing signal HSYNC. The image sensor LSI 1 applies an image signal to the signal-processor LSI 2 in sync with these synchronizing signals. Therefore, each of these signals SCLK, VSYNC, and HSYNC depends upon the system clock signal CLKIN.

[0043] Various kinds of parameters such as a parameter for brightening the whole or a part of an image and others, for example, are input and stored in the register 23 of the signal-processor LSI 2 via I^2C-Bus (I square C bus) I/F.

[0044] In the signal-processor LSI 2, the image processor 24 is a circuit that produces an image based on RGB signals and the sequencer 25 is a circuit that drives the image processor 24.

[0045] Furthermore, a clock designating signal CLK _ SEL is applied to the timing generator 13 of the image sensor LSI 1. The signal CLK _ SEL expressly informs the image sensor LSI 1 of the designation of clock frequency for operating the image sensor LSI 1. Namely, this is to input a control signal that indicates high and low clock frequencies to the image sensor LSI 1. Based on the signal CLK _ SEL, the timing generator 13 changes output timing for various kinds of control signals. Furthermore, a standby signal STANDBY is input into the timing generator 13.

[0046] Data such as a shutter speed, setting voltage for a regulator, designation of the scanning direction and others are input and stored in the register 14 of the image sensor LSI 1 via the three line serial interface 15.

[0047] In addition, the image sensor LSI 1 applies a valid signal VALID as a control signal to the timing generator 26 of the signal-processor LSI 2. The valid signal VALID shows that valid image data is output from the image sensor LSI 1. When this signal is activated, valid image data is output from the image sensor LSI 1 such that the signal-processor LSI 2 acknowledges that the data can be used for measuring the brightness and others.

[0048] Next, a structure of the image sensor LSI 1 is explained. FIG. 2 shows a circuit diagram of the image sensor LSI 1.

[0049] The sensor cell array 3 is a matrix type solid-state image-pickup element that includes cells S11 to Smn of m × n (m rows and n columns). One cell corresponds to one unit pixel. Each cell corresponding to each unit pixel includes a photo diode PDS and a MOS transistor PDTr that is an insulated gate type field effect transistor for detecting a light signal. The photo diode PDS includes an impurity diffused region and a well region where holes are generated in response to incident light. The well region is shared commonly with the MOS transistor PDTr for detecting a light signal and forms the gate region of the MOS transistor PDTr for detecting a light signal. The impurity diffused region of the photo diode PDS and the drain diffused region of the MOS transistor PDTr for detecting a light signal are formed integrally on the surface of the well region. The drain diffused region is formed as the outer circumference of a ring-shaped gate electrode. The source-diffused region is formed in the center of the ring-shaped gate electrode. Within the well region under the gate electrode and the peripheral of the source diffused region, a carrier pocket is formed like surrounding the source diffused region. The details

of the sensor structure are disclosed in the Japanese Patent Publication Laid-Open No. 11-195778.

[0050] In order to obtain a signal in response to an amount of light from the sensor cell array 3, a predetermined bias voltage is applied to the gate, source and drain of each cell in each of three states such as accumulation, reading out and clearing so as to obtain a signal in response to an amount of light. Simply stated, at the time of the accumulation state, holes generated in response to an amount of incident light to the photo diode PDS are stored in the carrier pocket. At the time of the reading out state, a signal voltage is read out based on accumulated holes. A read signal voltage corresponds to the difference between the gate voltage and threshold values varying in response to an amount of received light. At the time of the clearing state, the booster 7 boosts the source voltage of the MOS transistor PDTr for detecting a light signal to a predetermined value. Furthermore, the gate voltage is boosted to a predetermined value by coupling capacitance between the ring gate and the source so as to turn the MOS transistor PDTr for detecting a light signal "on" and form a channel under the ring gate. Therefore, the drain voltage becomes a value equivalent to the source voltage (when the drain voltage VD=VG-Vth and the gate voltage VG is sufficiently higher than the source voltage). Thus, the depletion layers under the source, channel and drain are spread out so as to sweep the accumulated holes out toward the substrate and exclude residual charges such as holes. After clearing, offset voltage including a noise component is read out and the difference between a signal voltage and the offset voltage is taken out so as to obtain an image signal. The above operation is executed for each cell and an image signal is obtained so as to obtain the two-dimensional image signal. A bias condition, namely a bias voltage applied to the gate, source and drain of each cell in each state is described below.

[0051] The second shift register 4 is a circuit that designates a line for clearing an image signal. Shift data AV applied to a line for clearing an image signal, a shift clock signal VCLK _ ASR applied to a line for clearing an image signal and a reset signal VSFRA _ RST are input to the second shift register 4. The second shift register 4 outputs a selection signal, VSA 1 to VSAm, which selects a line for clearing an image signal, which selects a line where accumulated charges are cleared in the sensor cell arrays 3 in a matrix.

[0052] The first shift register 5 is a circuit that designates a line for reading an image signal. Shift data BV applied to a line for reading an image

signal, a shift clock signal VCLK_BSR applied to a line for reading an image signal and a reset signal VSFRB_RST applied to shift register are input to the first shift register 5. The first shift register 5 outputs a signal, VSB 1 or VSBm, for selecting a line for reading an image signal, which selects a line where signal voltage is read out in the sensor cell arrays 3 comprising a matrix.

[0053] The shift data AV and the shift data BV are given at the timing determined by shutter speed data such that the second shift register 4 and the first shift register 5 output selecting signals in order. In other words, the shift data BV is produced at predetermined timing with respect to the vertical synchronizing signal VSYNC. On the other hand, the phase relationship between the shift data BV and the shift data AV is determined by shutter speed. While maintaining such phase relationship, the second shift register 4 and the first shift register 5 output a selecting signal in order. In addition, as described below, when a line for reading an image signal and a line for clearing an image signal exist in one frame, two lines in the sensor array are designated and selected.

[0054] The vertical drive circuit 6 includes two AND circuits 31 and 32, an OR circuit 33, a buffer circuit 34 and a drain gate voltage supply circuit VC1i ("i" is any one from 1 to m which is the same as follows) in every line. One AND circuit 31 receives the signal VSAi that selects a line for clearing an image signal and an enabling signal CLS that selects a line for clearing an image signal. The other AND circuit 32 receives the signal VSBi that selects a line for reading an image signal and an enabling a signal VSM that selects a line for reading an image signal and executes three operations such as reading a signal out, clearing it and reading a noise out. The OR circuit 33 receives a signal that is output from each of the AND circuits 31 and 32 and a signal VGUP for selecting all lines at the time of accumulation. The buffer circuit 34 receives a signal that is output from the OR circuit 33. An output signal from each buffer circuit 34 is supplied as a signal VSCi for selecting a line to the drain gate voltage supply circuit VC1i.

[0055] The drain gate voltage supply circuit VC1i receives the signal VSCi for selecting a line, an accumulation-enabling signal SDI, a reading-out enabling signal SDR 2 and a clearing pulse signal CL. The drain gate voltage supply circuit VC1i selects and outputs voltage that is applied to the gates and drains of all cells on a corresponding line. In other words, the drain gate voltage supply circuit VC1i applies a drain voltage VPDi and a gate voltage VPGi to

each cell on each line. The details of this drain gate voltage supply circuit VC1i are described below.

[0056] The source voltage supply circuit VC2h ("h" is any one from 1 to n that is the same hereafter) is arranged in every column of a matrix. The clearing pulse signal CL and a gate preset signal PR before clearing are input to the source voltage supply circuit VC2h. The source voltage supply circuit VC2h applies a source voltage VPSh to the sources of all cells of each column. The details of this source voltage supply circuit VC2h are described below.

[0057] A source line corresponding to each column is coupled to the line memory 9 that stores an accumulated signal and the line memory 10 that stores an offset signal via a switch SW1h. A data load signal LOAD applied to these line memories turns the switch SW1h "on".

[0058] The line memory 9 for an accumulated signal includes a selection circuit HSh corresponding to each column. Each selection circuit HSh includes a capacitor C2 that stores accumulated charge, a switch SW21 for reading-in, a switch SW22 for reset, and a switch SW23 for output.

[0059] The line memory 10 includes a selection circuit HNh corresponding to each column. Each selection circuit HNh includes a capacitor C3 that stores accumulated charge, a switch SW31 for reading-in, a switch SW32 for reset, and a switch SW33 for output. When a data load signal LOADS is input to the line memory 9, the SW21 is turned "on" by this signal, a voltage corresponding to an amount of light is given to the capacitor C2 from each source line, and charges corresponding to the voltage are stored in the capacitor C2. Pixel signals in one line that are selected by the first shift register 5 are stored in the line memory 9 in response to the data load signal LOADS.

[0060] A reset signal RESS applied to the line memory 9 turns a switch 22 "on" so as to apply a predetermined voltage VMPR to the capacitor C2 via the switch 22 just before reading a signal out. The voltage VMPR is a power potential 35 generated by the regulator 8.

[0061] Then, the switch SW23 of each selection circuit HSh of the line memory 9 for an accumulation signal is turned "on" sequentially by a selecting signal HSCANh from the horizontal shift register 11. The switch SW23 that was turned "on" outputs the voltage corresponding to charges stored in the capacitor C2, and pixel signals of one line selected by the first shift register 5 is output sequentially as the voltage output signal VOUTS via an output amplifier 36.

[0062] When a data load signal LOADN is input to the line memory 10, the switch SW31 connected to the line memory is turned "on" by this signal. Then, a voltage corresponding to offset component is given from each source line and charges corresponding to the voltage are stored in the capacitor C3. Pixel signals in one line that is selected by the first shift register 5 are stored in the line memory 10 in response to the data load signal LOADN. A reset signal RESN applied to the line memory turns the switch 32 "on" so as to apply the predetermined voltage VMPR to the capacitor C3 just before reading out an offset component signal. The voltage VMPR is a power potential 37 generated by the regulator 8.

[0063] Then, the horizontal shift register 11 turns the switch SW33 of each selection circuit HNh of the line memory 10 for an offset signal "on" sequentially. The switch SW33 that was turned "on" outputs the voltage corresponding to charges stored in the capacitor C3, and offset component signals of pixel signals of one line selected by the shift register 5 for reading a line out are output sequentially as the voltage output signal VOUTN via an output amplifier 38. Two voltage output signals VOUTS and VOUTN from the image sensor LSI 1 are input to the differential amplifier16 of the signal-processor LSI 2.

[0064] FIG. 3 is a circuit diagram which shows the drain gate voltage supply circuits VC 11 to VC 1m of FIG. 2. The drain gate voltage supply circuit VC1i includes NAND circuits, inverter circuits and transistors and outputs the gate voltage VPG and the drain voltage VPD in response to various input signals.

[0065] The clearing pulse signal CL, the accumulation-enabling signal SDI and the reading-out enabling signal SDR 2 are input to each drain gate voltage supply circuit VC1i. Furthermore, it produces bias voltages in FIG. 5 by using voltages VCCSGHR, VCCSGHI, VCCSDR and VCCSDI that are supplied and applies the bias voltages to the drain and gate of each sensor cell.

[0066] The sensor cell array 3 has the following states. Each of these states includes "accumulation", "reset (S)", "modulation (S)", "preset", "clearing", "reset (N)" and "modulation (N)" in detail, and an optical image is converted into an electrical signal so as to be output by repeating each of these states. The accumulation-enabling signal SDI is a low active signal showing an accumulation period. The reading-out enabling signal SDR 2 is a signal which is produced based on a signal SDR showing a period except the accumulation

period and becomes low active at the time of modulation, offset modulation and clearing. In addition, the signal VSCi for selecting a line is used for selecting a line for reading out an image signal and a line for clearing an image signal. The clearing pulse signal CL is set in a period for discharging residual charge such as accumulated holes.

[0067] In FIG. 3, it is assumed that the clearing pulse signal CL is an L level, and the signal VSCi for selecting a line becomes an H level. In this case, a P-channel MOS transistor T1 and an N-channel MOS transistor T2 are turned "on" and a P-channel MOS transistor T3 is turned "off". Then, the gate voltage VPGi becomes the voltage VCCSGHI or the voltage VCCSGHR. In addition, the P-channel MOS transistor T1 is an enhancement type and the N-channel MOS transistor T2 is a depletion type MOS transistor.

[0068] On the contrary, when the clearing pulse signal CL is an H level and the signal VSCi for selecting a line are an L level, the transistors T1 and T2 are turned "off" and the transistor T3 is turned "on". In this case, the gate voltage VPGi becomes a low level. In addition, when the clearing pulse signal CL and the signal VSCi for selecting a line are H level, the transistors T1, T2 and T3 are turned "off" and the gate becomes a floating state.

[0069] In addition, when the clearing pulse signal CL is an L level or the signal VSCi for selecting a line is an L level, an N-channel MOS transistor T5 is turned "on". The source of the transistor T5 for each line is commonly connected to form a COM node. When the transistor T5 is turned "on", the drain of each line is connected to the COM node and becomes a floating state. In the case when the transistor T5 is the "on" state, and when the accumulation-enabling signal SDI is an L level, a P-channel MOS transistor T6 and an N-channel MOS transistor T7 are turned "on" and the drain voltage VPDi becomes the voltage VCCSDI. In the case when the transistor T5 is the "on" state, and when the reading-out enabling signal SDR2 is an L level, the P-channel MOS transistor T4 is turned "on" and the drain voltage VPDi becomes the voltage VCCSDR. In the case when only the transistor T5 among transistors T4 to T7 is the "on" state, all drains are connected to COM node that is a floating state to be HiZ.

[0070] In addition, the transistor T1 receives the voltage VCCSGHI when the accumulation-enabling signal SDI is an L level, and receives the voltage VCCSGHR when the signal SDR is an L level.

[0071] Namely, the circuit of FIG. 3 obtains the states described in the following Table 1. Here, only H level and L level of signals which are paid attention to are shown in Table 1.

[0072] Table 1

VSCi	CL	SDI	SDR 2	VPGi
L	L			L (GND)
L	H			L (GND)
H	L	L		VCCSGHI
H	L		L	VCCSGHR
H	H			Floating
VSCi	CL	SDI	SDR 2	VPDi
L		L		VCCSDI
	L	L		VCCSDI
L			L	VCCSDR
	L		L	VCCSDR
	L	H	H	HiZ

[0073] FIG. 4A is a circuit diagram of the source voltage supply circuits VC21 to VC2n shown in FIG. 2. The source voltage supply circuit VC2h includes capacitors and transistors and outputs the source voltage VPSh in response to various kinds of input signals.

[0074] FIG. 4B shows a circuit that produces signals S1, S2, S3 and S4 shown in FIG.4A.

[0075] The signals S1 to S3 that are the inverted signals of the clearing pulse signal CL and the signal S4 that is a positively inverted signal of the gate preset signal PR are input to the source voltage supply circuit VC2h. Further, it produces the SOURCE bias voltage shown in FIG.5 by using signals VCCSDB and VCCVPS that are supplied and applies it to the source of each sensor cell.

[0076] In FIG.4B, the signals S1 to S3 are inverted signals of the clearing pulse signal CL and the signal S4 that is a positively inverted signal of the gate preset signal PR is a signal having the same logic level of the gate preset signal PR before clearing. When both the clearing pulse signal CL and the gate preset signal PR before clearing are L levels, the signals S1 to S3 are an H level and the signal S4 is an L level. Therefore, N-channel MOS

transistors T11 and T13 are "on", P-channel MOS transistors T12 and T14 are "off" and an N-channel MOS transistor T15 is "off". Namely, in this case, the transistors T14 and T15 are "off" such that the source voltage supply circuit VC2h does not supply the source voltage. At this time, a voltage value at the point ND1 is ground level (GND) and a voltage value at the point ND2 is VCCSDB.

[0077] In addition, the signals S1 to S3 and the signal S4 are H levels when the clearing pulse signal CL is an L level and the gate preset signal PR before clearing is an H level. Therefore, the transistors T11, T13, and T15 are "on", and the transistors T12, and T14 are "off". Namely, in this case, the source voltage VPSh becomes the voltage VCCVPS, the voltage value at the point ND1 is a ground level (GND) and a voltage value at the point ND2 is VCCSDB. Therefore, the capacitor C1 is charged to the voltage VCCSDB during this time.

[0078] In addition, when the clearing pulse signal CL is an H level and the gate preset signal PR before clearing is an L level, the signals S1 to S4 are L levels. Therefore, the transistors T11, T13, and T15 are "off", and the transistors T12, and T14 are "on". Namely, in this case, the voltage at the point ND2 becomes the source voltage VPSh. If the voltage of the capacitor C1 is charged to be the VCCSDB just before this case, the voltage value at the point ND1 becomes the voltage VCCSDB by turning the transistor T12 "on" such that the voltage at the point ND2 becomes VCCSDBx2.

[0079] Namely, the circuit of FIG. 4 obtains the states of the following Table 2.

[0080] Table 2

	CL	PR	VPSh
1)	L	L	Voltage is not supplied
2)	L	H	VCCVPS
3)	H	L	If it is just after state of 2) VCCSDBx2

[0081] FIG. 5 is a diagram for explaining a bias voltage applied to the sensor cell.

[0082] FIG. 5 shows the voltage values of the gate voltage, source voltage and drain voltage of each cell in each state. In addition, in FIG. 5, these

are divided into states of "accumulation", "reset (S)", "modulation (S)", "preset", "clearing", "reset (N)" and "modulation (N)" in terms of bias voltages.

[0083] In FIG. 5, GATE is a gate voltage of a cell that includes two states such as a selected state and a non-selected state. SOURCE is a source voltage of a cell. DRAIN is a drain voltage of a cell that includes two states such as a selected state and a non-selected state.

[0084] At first, the case of an accumulation state is described.

[0085] When the state of "accumulation" (it is referred to as accumulation state hereafter), all cells in a cell array are in a selected state and a voltage of which value is the VCCSGHI is applied to the gate. At the time of the accumulation state, there is no cell in the non-selected state. At the time of the accumulation state, the source does not receive the bias voltage from the source voltage supply circuit VC2h, but the gate receives the voltage of VCCSGHI and the MOS transistor PDTr for detecting a light signal is turned "on" such that the path between the source and the drain becomes a conductive state and the source becomes the drain voltage (VCCSDI) while in the accumulation state.

[0086] Next, the state of "reset (S)" (it is abbreviated with RESS state hereafter) is described.

[0087] In the case of a cell with a selected state, at the time of the RESS state, the voltage of which value is Lo (L level) is applied to the gate. At the time of the RESS state, the voltage of which value is VMPR is applied to the source.

[0088] In the case of a cell with a selected state, at the time of the RESS state, the voltage Lo is applied to the gate and the MOS transistor PDTr for detecting a light signal is turned "off" such that the path between the source and the drain becomes a non-conductive state and the drain becomes high impedance (HiZ).

[0089] In addition, in the case of a cell with a non-selected state, at the time of the RESS state, the voltage of which value is Lo (L level) is applied to the gate. When a certain cell is a non-selected state and the state is the RESS state, the drain becomes HiZ.

[0090] While in the state of "modulation (S)" (it is abbreviated with LOADS state hereafter), in the case of a cell with a selected state, the voltage of which value is VCCSGHR is applied to the gate. In the case of a cell with a selected state, the voltage of which value is VCCSDR is applied to the drain

and the voltage of which value is (VCCSGHR-VthS) is applied to the source. In the case of the LOADS state, it is necessary to apply the bias voltage having the relationship of (VCCSGHR <VCCSDR).

[0091] In addition, in the case of a cell with a non-selected state, at the time of the LOADS state, the voltage of which value is Lo is applied to the gate and the voltage of which value is VCCSDR is applied to the drain.

[0092] Next, the state of "preset" (it is abbreviated with the PR state hereafter) is described.

[0093] In the case of a cell with a selected state, at the time of the PR state, the voltage of which value is VCCSGHR is applied to the gate. At the time of the PR state, the voltage of which value is VCCVPS is applied to the source. In the case of a cell with a selected state, at the time of the PR state, the MOS transistor PDTr for detecting a light signal is turned "on" such that the drain voltage becomes the same voltage of the source.

[0094] In addition, in the case of a cell with a non-selected state, at the time of the PR state, the voltage of which value is Lo is applied to the gate and the voltage of the drain becomes VCCVPS. In a line where VSCi is a Lo level (= a non-selected line), the transistor T5 is turned "on" such that each line is connected to the common node (COM node) and the COM node becomes HiZ.

[0095] At the time of the state of "clearing" (it is abbreviated with the CL state hereafter), in the case of a cell with a selected state, the voltage of which value is (VCCSDBx2) is applied to the source, and the MOS transistor PDTr for detecting a light signal is turned "on" such that the voltage of the drain becomes the same voltage of the source. As a result, the voltage of which value is (VCCSGHR+VCCSDBx2) is applied to the gate.

[0096] In addition, in the case of a cell with a non-selected state, at the time of the CL state, the voltage of which value is Lo is applied to the gate and the voltage of which value is VCCSDR is applied to the drain.

[0097] Next, the state of "reset (N)" (it is abbreviated with the RESN state hereafter) is described.

[0098] In the case of a cell with a selected state, at the time of the RESN state, the voltage of which value is Lo is applied to the gate. At the time of the RESN state, the voltage of which value is VMPR is applied to the source. In the case of a cell with a selected state, the drain becomes HiZ at the time of the RESN state.

[0099] In addition, in the case of a cell with a non-selected state, the voltage of which value is Lo is applied to the gate at the time of the RESN state. In the case of a cell with a non-selected state, the drain becomes HiZ at the time of the RESN state.

[00100] Here, during a period when the clearing pulse signal CL is an L level, the N-channel MOS transistor T5 of FIG. 3 is turned "on". Therefore, even in the RESS state, the N-channel MOS transistor T5 is turned "on" and the drain is connected to the COM node. The reading-out enabling signal SDR 2 becomes an H level while in the states of RESS and RESN so as to turn the P-channel MOS transistor T4 "off" such that the COM node becomes floating state.

[0100] While in the state of "modulation (N)" (it is abbreviated with LOADN state hereafter), the voltage of which value is VCCSGHR is applied to the gate in the case of a cell with a selected state. At the time of the LOADN state, the voltage of which value is VCCSDR is applied to the drain and the voltage of which value is (VCCSGHR-VthN) is applied to the source.

[0101] In addition, in the case of a cell with a non-selected state, at the time of the LOADN state, the voltage of which value is Lo is applied to the gate and the voltage of which value is VCCSDR is applied to the drain.

[0102] Similarly to the LOADS state, at the time of the LOADN, the transistor T5 of FIG. 3 is turned "on" such that the drain is connected to the COM node (= HiZ).

[0103] FIG. 6 shows a diagram for explaining a line for reading out an image signal and a line for clearing an image signal of a sensor.

[0104] As shown in FIG. 6, in a matrix of m × n, each line from the first line to the mth line is scanned sequentially. A line for reading out an image signal is a line where a signal corresponding to quantity of light is read out, and a line for clearing an image signal is a line where charges stored in each cell are cleared. Each line is scanned sequentially from the first line such that each cell in a line that is cleared based on the signal for selecting a line for clearing an image signal produces holes corresponding to an amount of received light after clearing. After clearing, time when the line has been read out by the signal VSBi for selecting a line for reading out an image signal is time for the exposure. The exposure time is proportional to the number of line "d1" between line for reading out an image signals and line for clearing an image signals and can be changed by setting of a shutter speed. In other word, this time can be

changed by setting the range from 1H (H means the number of horizontal lines hereafter) to mH (or 1 frame + more than 1 H may be enough).

[0105] FIG. 7 is a timing chart showing timing of the vertical synchronizing signal VSYNC and the horizontal synchronizing signal HSYNC.

[0106] The vertical synchronizing signal VSYNC is a timing pulse produced every period t1 and its length is t2. The horizontal synchronizing signal HSYNC is a timing pulse produced every period t3 and its length is t4. The vertical synchronizing signal VSYNC and the horizontal synchronizing signal HSYNC are applied to the image sensor LSI 1 from the timing generator 26 of the signal-processor LSI 2.

[0107] The first shift register 5 outputs the signal VSBi for selecting a line for reading out an image signal sequentially when the vertical synchronizing signal VSYNC is applied. Within a period t1 after applying the vertical synchronizing signal VSYNC, a plurality of the horizontal synchronizing signals HSYNC are output by the number of lines (= m) in the sensor cell array 3. Furthermore, within the period t4 when the horizontal synchronizing signal HSYNC is output and the VGUP is L, there exists a period when the above-mentioned reading a signal component out, clearing, and reading the offset component out are executed. The period when the VGUP is L is set to be a predetermined period within H blanking period. The H blanking period is explained in detail by using FIG. 9 later.

[0108] Within a period t5 after the period t4 within the period t3, "n" number of signal components and offset components, namely the analog signals VOUTS and VOUTN are output.

[0109] Next, the circuit structure of the timing generator (it is referred to as TG hereafter) 13 of the image sensor LSI 1 is described referring to FIG. 8.

[0110] FIG. 8 is a circuit block diagram showing a structure of the TG 13 of the image sensor LSI 1 of FIG. 1.

[0111] The TG 13 includes a serial control block 71, a master timing control block 72, a sensor register block 73, a shutter control unit (a control unit for the upper limitation of a shutter speed) 74, a frame control unit 75, an H·V counter 76, a vertical scanning control block 77, a horizontal scanning control block 78, and an analog control block 79.

[0112] To and from the serial control block 71, a three line serial I/F signal that is an interface signal between the serial control block 71 and the register 14 of the signal-processor LSI 2 is input and output.

[0113] To the master timing control block 72, the sensor drive clock signal SCLK, the horizontal synchronizing signal HSYNC and the vertical synchronizing signal VSYNC are input from the TG26 of the signal-processor LSI 2. In addition, the clock designating signal CLK _ SEL and the standby signal STANDBY are input to the TG13 inputs from the signal-processor LSI 2.

[0114] The serial control block 71 receives setting data of a shutter speed written to the register 23 of the signal-processor LSI 2, setting data of the regulator 8 and system clock information as serial I/F signals. Based on these data, it outputs write data, write address and a write strobe signal WR and applies these data and the signal to the sensor register block 73.

[0115] In response to the above input signals, the sensor register block 73 outputs a line shutter speed setting signal, a frame shutter speed setting signal, a frame mode setting signal, a clearing pulse-width control setting signal, a signal for setting the number of applying clearing pulses, a gain setting signal and a regulator voltage setting signal.

[0116] On the other hand, the master timing control block 72 outputs a pixel clock signal, a horizontal reset pulse signal, a vertical reset pulse signal and a reset signal based on the above-mentioned various input signals.

[0117] To the shutter control unit (the control unit for the upper limitation of a shutter speed) 74, the line shutter speed setting signal and the frame shutter speed setting signal from the sensor register block 73 are input. The shutter control unit 74 outputs line shutter speed data and frame shutter speed data.

[0118] To the frame control unit 75, the pixel clock signal, the vertical reset pulse signal and the reset signal from the master timing control block 72 and the above-mentioned standby signal STANDBY are input. The frame control unit 75 outputs a frame counted value, frame control data and a valid (VALID) control signal.

[0119] In addition, to the H·V counter 76, the pixel clock signal, the horizontal reset pulse signal, the vertical reset pulse signal and the reset signal from the master timing control block 72 are input. The H·V counter 76 outputs a line counted value and a pixel counted value.

[0120] To the vertical scanning control block 77, the line shutter speed data and the frame shutter speed data from the shutter control unit 74, the frame counted value, the frame control data and the valid (VALID) control signal from the frame control unit 75, the clearing pulse-width control setting signal

and the signal for setting the number of the applying clearing pulse from the sensor register block 73, the pixel clock signal, the reset signal and the clock designating signal CLK _ SEL from the master timing control block 72 and the line counted value and the pixel counted value from the H·V counter 76 are input.

[0121] Further, the vertical scanning control block 77 outputs the shift data AV applied to a line for clearing an image signal, the shift clock signal VCLK _ ASR applied to a line for clearing an image signal, the reset signal VSFRA _ RST applied to a shift register for clearing a line, the enabling signal CLS for selecting a line for clearing an image signal, the shift data BV applied to a line for reading an image signal, a shift clock signal VCLK _ BSR applied to a line for reading out image signal, the reset signal VSFRB _ RST applied to shift register for reading out an image signal, the enabling signal VSM that selects a line for reading an image signal, the signal VGUP for selecting all lines at the time of accumulation, the accumulation-enabling signal SDI, the reading-out enabling signal SDR2, the gate preset signal PR before clearing and the clearing pulse signal CL.

[0122] To the horizontal scanning control block 78, the valid (VALID) control signal from the frame control unit 75, the line counted value and the pixel counted value from the H·V counter 76, the clearing pulse-width control setting signal from the sensor register block 73, and the pixel clock signal, the reset signal and the clock designating signal CLK _ SEL from the master timing control block 72 are input.

[0123] The horizontal scanning control block 78 outputs shift data AH for selecting a line memory, a shift clock signal CIN for selecting a line memory, an enabling signal HSC _ CK for selecting a line memory, the reset signal RESS, the data load signal LOADS, the reset signal RESN and the data load signal LOADN.

[0124] The above clock designating signal CLK _ SEL is a signal indicating high and low of frequency of the system clock signal CLKIN. This CLK _ SEL is applied to the vertical scanning control block 77 and the horizontal scanning control block 78. Each of control blocks 77 and 78 controls output timing of various driving signals for sensors output from each of control blocks 77 and 78 in response to H or L level of the clock designating signal CLK _ SEL.

[0125] To the analog control block 79, the valid (VALID) control signal from the frame control unit 75, the line counted value and the pixel counted

value from the H·V counter 76, the gain setting signal from the sensor register block 73, and the standby signal STANDBY are input. Further, the analog control block 79 outputs an analog amplifier gain control signal, a clock signal CDL for driving amplifier and a standby control signal.

[0126] Further, the valid (VALID) control signal from the frame control unit 75 is applied to the signal-processor LSI 2 from the TG 13 as the valid signal.

[0127] In addition, the regulator voltage setting signal from the sensor register block 73 and the standby control signal from the analog control block 79 are input to the regulator 8 for producing a bias of driving a sensor in the image sensor LSI 1 of FIG. 1.

[0128] The analog amplifier gain control signal and the clock signal CDL for driving an amplifier from the analog control block 79 becomes the control signal for the output amplifier 12 of the image sensor LSI 1 of FIG. 1.

[0129] FIG. 9 is a timing chart showing each signal of controlling photoelectric conversion of the sensor cell array 3. The sensor cell array 3 converts an optical image to an electrical signal and output it by repeating each state of "accumulation", "reset (S)", "modulation (S)", "preset", "clearing", "reset (N)" and "modulation (N)". FIG. 9 shows a manner of each signal while in these states. The sensor cell array 3 works with a predetermined frame rate where the vertical synchronizing signal VSNYC and the horizontal synchronizing signal HSYNC in FIG. 7 are referred to as a unit time.

[0130] In the example of FIG. 9, regarding a certain line count signal ROWCT, the HSYNC is an L level during the term when a pixel clock signal PXLCT is from 1 to 80. Further, the state of LOADS (reset (S) + modulation (S)) is assigned during the term when the PXLCT is from 5 to 26, the state of CL (preset + clearing) is assigned during the term when the PXLCT is from 27 to 44, and the state of LOADN (reset (N) + modulation (N)) is assigned during the term when the PXLCT is from 45 to 63.

[0131] In addition, each control signal is produced by the TG 13. The TG 13 includes a logic circuit. This logic circuit is automatically designed by using a designing system HDL (Hardware Description Language) such as Verilog-HDL, VHDL and others.

[0132] At first, the accumulation state is described.

[0133] This accumulation period is a period except a predetermined period in the H blanking period shown in FIG. 7 (from the 5th pixel to the 63rd

pixel in FIG. 9). In the accumulation period, all pixels become the accumulation state. In this period, the signal VGUP for selecting all lines at the time of accumulation is an H level and the accumulation-enabling signal SDI and the clearing pulse signal CL are an L level. As shown in FIG. 2, when the signal VGUP for selecting all lines at the time of accumulation is an H level, all of the signal VSCi for selecting a line become an H level and the gate voltage VPGi becomes VCCSGHI as shown in Table 1 which indicates the operation of the drain gate voltage supply circuit VC1i .

[0134] In addition, the drain voltage VPDi becomes the voltage VCCSDI. In addition, the gate preset signal PR before clearing is an L level during this period and the source voltage supply circuit VC2h does not supply a source voltage as shown in Table 2 which indicates the operation of the source voltage supply circuit VC2h. In this case, the voltage of the sources of all cells in a cell array becomes the drain voltage when the MOS transistor PDTr for detecting a light signal is turned "on".

[0135] The accumulation period is completed in the 5th pixel of the H blanking period and reading a signal out starts. In the period for reading a signal out (the periods for LOADS, CL, and LOADN), accumulation of holes based on an amount of received light is continued, but each cell is set to be a value different from that in the accumulation period. In addition, in the period for reading an image signal out, each cell is set to be an individual value at a line for clearing an image signal, a line for reading out an image signal or a non-selected line.

[0136] At first, the reset (s) state is described. As shown in FIG. 9,even in this period, a setting which is in common for all cells is executed.

[0137] As shown in FIG. 9, the clearing pulse signal CL and the gate preset signal PR before clearing are L levels and the source voltage supply circuit VC2h does not supply the source voltage. During this period, the reset signal RESS is activated, and the switch SW22 of FIG. 2 is turned "on" such that the voltage of the end of the capacitor C2 which forms the line memory is charged to the VMPR. Furthermore, the data load signal LOADS and the data load signal LOAD are activated, the switch SW21 and the switch SW11 are turned "on" and the source line is initialized by the voltage VMPR.

[0138] On the other hand, the signal VGUP for selecting all lines at the time of accumulation varies from H to L and all of the signal VSCi for selecting a line is turned to be an L level. Therefore, as shown in Table 1, all of

the gate voltage VPSGi becomes an L (GND) level. In addition, the accumulation-enabling signal SDI is an H level and the SDR2 is also an H level, such that the drains of all cells are connected commonly (COM node) and the COM node becomes HiZ state since the T5 in FIG. 3 has been turned "on" as shown in Table 1.

[0139] Next, the modulation (s) state is described.

[0140] As shown in FIG. 9, the CL and PR keep L levels and the source voltage supply circuit VC2h does not supply a voltage to a source line. The voltage corresponding to a predetermined value set to each cell is output via the source line. Namely, regarding a line for clearing an image signal and non-selected line, the signal VSCi for selecting a line holds an L level and the gate voltage is an L (GND) level. In addition, the reading-out enabling signal SDR2 is also an L level such that the drain voltage VPDi becomes VCCSDR.

[0141] Regarding the line for reading out an image signal, the signal VSCi for selecting a line is an H level. The clearing pulse signal CL and the signal SDR are L levels such that the gate voltage VPGi is VCCSGHR. The drain voltage VPDi is VCCSDR. Thus, the source voltage VPSi shows voltage (VCCSGHR-VthS) thereby. In addition, VthS varies depending on accumulated holes. The voltage of a source line (VCCSGHR-VthS) is stored in each capacitor C2 which forms the line memory via the switch SW21.

[0142] Next, in order to process correlation double sampling, the CL state for removing (clearing) holes stored in each cell of the line for reading out an image signal is set. It is necessary to apply extremely high voltage to the gate in order to remove holes. This high voltage is obtained by setting the preset state before the clearing state and using a booster. In addition, each cell is cleared at the same time when clearing a line for reading out an image signal simultaneously.

[0143] At first, in the preset state, regarding a line for reading out an image signal and a line for clearing an image signal, the signal VSCi for selecting a line is an H level. The clearing pulse signal CL and the signal SDR are L levels such that the gate voltage VPGi is VCCSGHR. In addition, regarding a non-selected line, the signal VSCi for selecting a line is an L level such that the gate voltage is an L (GND) level.

[0144] In addition, the clearing pulse signal CL is an L level and the gate preset signal PR before clearing is H such that the voltage for all source lines VPSh is reset to the voltage VCCVPS (0V, for example) as shown in Table

2. In addition, the voltage VCCSDB is charged to the capacitor C1 of FIG. 4, and the point ND2 becomes the voltage VCCSDB. In addition, the accumulation-enabling signal SDI and the reading-out enabling signal SDR2 are H levels such that the drain voltage becomes the same level of the source voltage since the MOS transistor PDTr for detecting a light signal is turned "on".

[0145] Next, in the clearing state, the gate preset signal PR before clearing varies from an H level to an L level and the clearing pulse signal CL varies from an L level to an H level. In this case, a source line changes to the voltage VCCSDB x2 as shown in Table 2. In addition, regarding a line for reading out an image signal and a line for clearing an image signal, the clearing pulse signal CL and the signal VSCi for selecting a line are H levels such that the gate becomes a floating state, as shown in Table 1. Therefore, the gate voltage VPGi becomes (VCCSDB x2+VCCSGHR) by coupling capacitance of the source with the gate. In addition, the drain voltage of the MOS transistor PDTr for detecting a light signal becomes the same level of the source voltage since the MOS transistor is turned "on" similar to the preset state.

[0146] On the other hand, regarding a non-selected line, the gate voltage VPGi holds an L (GND) level, and the drain voltage VPDi becomes VCCSDR when the transistor T4 is turned "on".

[0147] Next, a state is shifted to the modulation (N) state via the reset (N) state. In these reset (N) state and modulation (N) state, signals almost similar to that of the reset (s) state and the modulation (s) state are set. Namely, in the reset (N) state, the reset signal RESN applied to line memory for an offset signal, the data load signal LOADN applied to line memory for an offset component accumulation signal are activated instead of the reset signal RESS applied to line memory for an accumulation signal and the data load signal LOADS applied to line memory for an accumulation signal, respectively. The switch SW32 is turned "on" thereby, and the capacitor C3 forming a line memory for reading a noise out is charged to the VMPR. Furthermore, the switch SW31 and the switch SW11 are turned "on", and a source line is initialized with the voltage VMPR.

[0148] In the modulation (N) state, the clearing pulse signal CL and the gate preset signal PR before clearing are L levels, and the source voltage supply circuit VC2h does not supply voltage to a source line. Regarding a line for clearing an image signal and a non-selected line, the signal VSCi for selecting a line is an L level and the gate voltage VPGi is L (GND). In addition,

the reading-out enabling signal SDR2 is also an L level such that the drain voltage VPDi becomes VCCSDR.

[0149] Regarding a line for reading out an image signal, the signal VSCi for selecting a line is an H level. The clearing pulse signal CL and the signal SDR are L levels such that the gate voltage VPGi is VCCSGHR. The drain voltage VPDi is VCCSDR. The source voltage VPSh shows the voltage (VCCSGHR - VthN) thereby. The voltage shown in the source is set to the cleared state just before such that it is corresponding to the offset component. The voltage of a source line (VCCSGHR-VthN) is stored in each capacitor C3 which forms a line memory via the switch SW31.

[0150] Thus, the signal component is stored in the capacitor C2 and the offset component is stored in the capacitor C3. The switches SW23 and SW33 are turned "on" in order by the selecting signal HSCANh from the horizontal shift register 11 such that the voltage stored in the capacitors C2 and C 3 are output as VOUTS and VOUTN via the output amplifiers 36 and 38, respectively.

[0151] Next, a modified example of the drain gate voltage supply circuit VC11 or VC1m is explained referring to Fig. 10

[0152] A drain gate voltage supply circuit VC1i shown in Fig. 10 includes a NOR circuit, a NAND circuit, an inverter, transistors and outputs a drain voltage VPD and a gate voltage VPG depending on various input signals. The circuit of Fig. 10 is different from that in Fig. 3 in a manner where three different voltages are supplied as the gate voltage VPGi.

[0153] The clearing pulse signal CL, the accumulation enabling signal SDI and the enabling signal SDR 2 are input to the drain gate voltage supply circuit and each bias voltage is applied to the drain and gate of each sensor cell by using supplied voltages VCCSGHI, VCCSGHR, VCCSGHPR, VCCSDR and VCCS DI.

[0154] In Fig. 10, it is assumed that the clearing pulse signal CL is an L level, and the line-selecting signal VSCi is an H level. In this case, an N channel MOS transistor T 22 is turned "on" or an N channel MOS transistor T 23 is turned "off".

[0155] When VGUP is an H level, a P-channel MOS transistor T 28 is turned "on" such that the gate voltage VPGi becomes the voltage VCCSGHI. In addition, when SDR 2 or CL is an L level, a P-channel MOS transistor T 28 is turned "on" and the gate voltage VPGi becomes VCCSGHI. Furthermore, if PR

and VSCi are H levels, a P-channel MOS transistor T 21 is turned "on" and the gate voltage VPGi becomes VCCSGHPR.

[0156] On the contrary, when the clearing pulse signal CL is an H level and the line-selecting signal VSC is an L level, the transistor T 23 is turned "off" and the transistor T 22 is turned "on". In this case, gate voltage VPGi becomes low voltage.

[0157] In addition, when the clearing pulse signal CL and the line numerical signal VSCi are H levels, the transistor T 23 is turned "off" and the gate becomes a floating state.

[0158] In addition, when the clearing pulse signal CL is an L level or the line-selecting signal VSC is an L level, the N channel MOS transistor T 25 is turned "on". In this case, an N channel MOS transistor T 27 is tuned "on" when the accumulation-enabling signal SDI is an L level, too, and the drain voltage VPDi becomes the voltage VCCS DI. In addition, when the transistor T 25 is turned the "on" state and the reading -out enabling signal SDR 2 is an L level, the P-channel MOS transistor T 24 is turned "on", drain voltage VPDi becomes the voltage VCCSDR. In addition, when only the transistor T 25 of transistors T 24 to T 27 is turned "on", the drains of all cells are commonly connected (COM node) such COM node becomes the Hiz state.

[0159] As described above, the gate voltage VPGi that is applied to the gate of each cell of the sensor cell array 3 is selected from three power sources and supplied.

[0160] Therefore, in each state, the voltages applied to the gates for all cell are different such that it is possible to boost the gate voltage at the time of reading out. Thus, an image with high quality can be output.

[0161] According to the above-mentioned preferred embodiments, an image-processing device that outputs image with high quality since an appropriate gate voltage is applied, can be realized.